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1 Geometric programming: a programming approach to geometric design 97%
Alberto Paoluzzi , Valerio Pascucci , Michele Vicentino
ACM Transactions on Graphics (TOG) July 1995
Volume 14 Issue 3
This article presents a functional programming approach to geometric design with embedded polyhedral complexes. Its main goals are to show the expressive power of the language as well as its usefulness for geometric design. The language, named PLASM (the Programming LAnguage for Solid Modeling), introduces a very high level approach to “constructive” or “generative” modeling. Geometrical objects are generated by evaluating some suitable language expressions. Because ...

2 Gate sizing with controlled displacement 90%
Wei Chen , Cheng-Ta Hsieh , Massoud Pedram
Proceedings of the 1999 international symposium on Physical design April 1999

3 Concurrent logic restructuring and placement for timing closure 88%
Jinan Lou , Wei Chen , Massoud Pedram
Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design
November 1999
In this paper, an algorithm for simultaneous logic restructuring and placement is presented. This algorithm first constructs a set of super-cells along the critical paths and then generates the set of non-inferior re-mapping solutions for each supercell. The best mapping and placement solutions for all super-cells are obtained by solving a generalized geometric programming (GGP) problem. The process of identifying and optimizing the critical paths is iterated until timing closure is achieve ...

4 Model order reduction: Realizable parasitic reduction using generalized Y-? transformation 87%

Zhanhai Qin , Chung-Kuan Cheng

Proceedings of the 40th conference on Design automation June 2003

We propose a realizable RCLK-in-RCLK-out parasitic reduction technique. The method employs generalized Y-? transformation. In our method, admittances are kept in their original rational forms of s, and their orders are reduced by truncating high-order terms. Therefore reduced admittances match the low-order terms in exact admittances. First-order realization of admittances is guaranteed, and higher-order realization is achieved by template optimization using Geometric Programming. The algor ...

5 On translating geometric solids to functional expressions 82%

Omid Banyasad , Philip T. Cox

Proceedings of the 5th ACM SIGPLAN international conference on Principles and practice of declaritive programming August 2003

Language for Structured Design (LSD)is a high level, visual, logic programming language for design of structured objects. LSD combines the design and programming activities in a homogeneous programming/design environment by extending Lograph, a visual logic programming language, with the notion of solids and operations on them. At the back-end, however, a solid modeling kernel for maintaining low level description of solids and operations is required.In this paper, we report on our progress towa ...

6 Design of pipeline analog-to-digital converters via geometric programming 82%

Maria del Mar Hershenson

Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design November 2002

In this paper we present a method for the design of analog-todigital converters (ADCs). This method computes the sizes of the different components (transistors, capacitors, etc.) in a predefined ADC topology so that the design specifications are met in the desired process technology.The method is based on formulating the ADC design constraints such as specifications on power, signal-to-noise ratio (SNR), area, and sampling frequency in special convex form in terms of the component sizes of the A ...

7 Design and optimization of LC oscillators 82%

Maria del Mar Hershenson , Ali Hajimiri , Sunderarajan S. Mohan , Stephen P. Boyd , Thomas H. Lee

Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design November 1999

We present a method for optimizing and automating component and transistor sizing for CMOS LC oscillators. We observe that the performance measures can be formulated as posynomial functions of the design variables. As a result, the LC oscillator design problems can be posed as a geometric program, a special type of optimization problem for which very efficient global optimization methods have recently been developed. The synthesis method is ...

8 Optimization of inductor circuits via geometric programming 82%

Maria del Mar Hershenson , Sunderarajan S. Mohan , Stephen P. Boyd , Thomas H. Lee

Proceedings of the 36th ACM/IEEE conference on Design automation conference June 1999

9 GPCAD: a tool for CMOS op-amp synthesis 82%
Maria del Mar Hershenson , Stephen P. Boyd , Thomas H. Lee
Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design November 1998

10 A perspective for the study of social and urban systems 80%
Jerome L. Uhrig
Proceedings of the fourth annual conference on Applications of simulation December 1970
An approach to the study of large and complex systems, in which the complementary properties of structural and behavioral characterizations are used to provide a unified framework to meet the needs of design documentation, mathematical analysis, and simulation, is discussed in the light of its applicability to social and urban systems.

11 Designing linear storage hierarchies so as to maximize reliability subject to cost and performance constraints 80%
K. S. Trivedi
Proceedings of the 7th annual symposium on Computer Architecture May 1980
A geometric programming model is proposed to determine the optimal design of the CPU and its matching storage hierarchy. The objective function is the maximization of system reliability subject to performance and budgetary limitations. Examples illustrating the use of the model are presented.

12 Analog design space exploration: Efficient description of the design space of analog circuits 80%
Maria del Mar Hershenson
Proceedings of the 40th conference on Design automation June 2003
In this paper we present a method for determining the feasible set of analog design problems and we propose an efficient method for their verification. The verification method presented relies on the formulation of the analog circuit design problem as a convex optimization problem in both the design variables and the performance specifications. Since the design is convex not only in the design variables but also in the specification parameters, we observe that the feasible sets are convex and po ...

13 CAD: Synthesis of continuous-time filters and analog to digital converters by integrated constraint transformation, floorplanning and routing 80%
Hua Tang , Hui Zhang , Alex Doboli
Proceedings of the 13th ACM Great Lakes Symposium on VLSI April 2003
This paper describes a layout-aware analog synthesis methodology. The methodology includes parameter exploration and classification, parameter domain pruning and sampling, and identification of parameter dependencies. The optimization process executes a combined constraint transformation, floorplanning and global routing. The paper presents results for a high frequency continuous-time filter, and two ?? ADCs. Compared to similar work, the methodology is more flexible in handling new de ...

14 Analog synthesis & design methodology: An efficient optimization--based technique to generate posynomial performance models for analog integrated circuits 80%
Walter Daems , Georges Gielen , Willy Sansen
Proceedings of the 39th conference on Design automation June 2002
This paper presents an new direct--fitting method to generate posynomial response surface

models with arbitrary constant exponents for linear and nonlinear performance parameters of analog integrated circuits. Posynomial models enable the use of efficient geometric programming techniques for circuit sizing and optimization. The automatic generation avoids the time--consuming nature and inaccuracies of handcrafted analytic model generation. The technique is based on the fitting of posynomial mode ...

15 Closed form solutions to simultaneous buffer insertion/sizing and wire sizing 80%
Chris Chu , D. F. Wong
ACM Transactions on Design Automation of Electronic Systems (TODAES) July 2001
Volume 6 Issue 3
In this paper, we consider the delay minimization problem of an interconnect wire by simultaneously considering buffer insertion, buffer sizing and wire sizing. We consider three cases, namely using no buffer (i.e., wire sizing alone), using a given number of buffers, and using the optimal number of buffers. We provide elegant closed form optimal solutions for all three problems. These closed form solutions are useful in early stages of the VLSI design flow such as logic synthesis and floo ...

16 A polynomial time optimal algorithm for simultaneous buffer and wire sizing 80%
C. C. N. Chu , D. F. Wong
Proceedings of the conference on Design, automation and test in Europe February 1998
An interconnect joining a source and a sink is divided into fixed-length uniform-width wire segments, and some adjacent segments have buffers in between. The problem we considered is to simultaneously size the buffers and the segments so that the Elmore delay from the source to the sink is minimized. Previously, no polynomial time algorithm for the problem has been reported in literature. In this paper, we present a polynomial time algorithm \mathit{SBWS}\ for the simultaneous buffer and wire si ...

17 Stack processing techniques in delayed-staging storage hierarchies 80%
Gabriel M. Silberman
Communications of the ACM November 1983
Volume 26 Issue 11

18 Sensitivity Analysis Procedures for Geometric Programs: Computational Aspects 80%
J. J. Dinkel , Mary S. Kochenberger , S. N. Wong
ACM Transactions on Mathematical Software (TOMS) March 1978
Volume 4 Issue 1

19 CYCLONE: automated design and layout of RF LC-oscillators 80%
C. De Ranter , B. De Muer , G. Van der Plas , P. Vancorenland , M. Steyaert , G. Gielen , W. Sansen
Proceedings of the 37th conference on Design automation June 2000
This paper presents an automated, layout-aware RF LC-oscillator design tool, called CYCLONE that delivers an accurate and optimal LC-oscillator design, from specification to layout. The tool combines the accuracy of device-level simulation and finite element analysis with the optimisation power of simulated annealing algorithms and is verified with experimental results.

20 Optimal Design of Linear Storage Hierarchies 80%
Kishor S. Trivedi , Timothy M. Sigmon
Journal of the ACM (JACM) April 1981
Volume 28 Issue 2

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Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design November 1999
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Proceedings of the 36th ACM/IEEE conference on Design automation conference June 1999

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Volume 4 Issue 1

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7 Macro-driven circuit design methodology for high-performance datapaths 77%
Mahadevamurty Nemani , Vivek Tiwari
Proceedings of the 37th conference on Design automation June 2000
Datapath design is one of the most critical elements in the design of a high performance microprocessor. However datapath design is typically does manually, and is often custom style. This adversely impacts the overall productivity of the design team, as well as the quality of the design. In spite of this, very little automation has been available to the designers of high performance datapaths. In this paper we present a new “macro-driven” approach to the design of datapath circ ...

8 GPCAD: a tool for CMOS op-amp synthesis 77%
Maria del Mar Hershenson , Stephen P. Boyd , Thomas H. Lee
Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design November 1998

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